Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (original) A locked loop, comprising:

a delay line having a first portion providing a variable amount of delay substantially independently of process, temperature and voltage variations and a second portion in series with said first portion and providing a variable amount of delay that substantially tracks changes in process, temperature, and voltage variations;

a control circuit for controlling the delay of said delay line;

a phase detector for producing signals for input to said control circuit; and

a feedback path for connecting an output of said delay line to an input of said delay line and to said phase detector.

2. (original) The locked loop of claim 1 wherein said first portion of said delay line has a small intrinsic delay and said second portion of said delay line has a higher intrinsic delay than said first portion.

3. (original) The locked loop of claim 1 wherein in said first portion of said delay line the delay is varied by varying the load and in said second portion of said delay line the delay is varied by selecting a desired signal path.

4. (original) The locked loop of claim 3 wherein the desired signal path is one of a slow path and a fast path.

5. (original) The locked loop of claim 3 wherein the desired signal path is one of a series path through an inverter or a parallel path through inverters.

6. (original) A locked loop, comprising:

a delay line having a first portion providing a variable amount of delay with little intrinsic delay and a second portion providing a variable amount of delay with a larger intrinsic delay;

a control circuit for controlling the delay of said delay line;

a phase detector for producing signals for input to said control circuit; and

a feedback path for connecting an output of said delay line to an input of said delay line and to said phase detector.

7. (original) The locked loop of claim 6 wherein the delay of said first portion of said delay line is substantially independent of process, temperature and voltage variations and wherein the delay of the second portion of the delay line substantially tracks changes in process, temperature and voltage variations.

8. (original) The locked loop of claim 6 wherein in said first portion of said delay line the delay is varied by varying the load and in said second portion of said delay line the delay is varied by selecting a desired signal path.

9. (original) The locked loop of claim 8 wherein the desired signal path is one of a slow path and a fast path.

10. (original) The locked loop of claim 8 wherein the desired signal path is one of a series path through an inverter or a parallel path through inverters.

11. (original) A locked loop, comprising:

a first circuit path having a stepwise variable capacitive load;

a second circuit path in series with the first circuit path and having a plurality of stages each having at least two paths;

a control circuit for controlling the amount of capacitance in said first circuit path and the number of stages in said second circuit path;

a phase detector for producing signals for input to said control circuit; and

a feedback path between an output of the second circuit path and an input of the first circuit path and said phase detector.

12. (original) The locked loop of claim 11 wherein said first circuit path has an intrinsic delay smaller than the intrinsic delay of said second circuit path.

13. (original) The locked loop of claim 11 wherein said first circuit path is substantially independent of process, temperature and voltage variations while said second circuit path substantially tracks changes in process, temperature and voltage.

14. (original) The locked loop of claim 11 wherein the two paths include a fast and a slow path.

15. (original) The locked loop of claim 11 wherein the two paths include a series path through an inverter and a parallel path through inverters.

16. (currently amended) A locked loop, comprising:

a first circuit path having a stepwise variable capacitive load ;

a second circuit path in series with said first circuit path and having a plurality of stages each having a variable amount of drive associated therewith;

a control circuit for controlling the amount of capacitance in said first circuit path and the number of stages in said second circuit path; and

a feedback path between an output of the second circuit path and an input of the first circuit path and said phase detector.

17. (original) The locked loop of claim 16 wherein said first circuit path has an intrinsic delay smaller than the intrinsic delay of said second circuit path.

18. (original) The locked loop of claim 16 wherein said first circuit path is substantially independent of process, temperature and voltage variations while said second circuit path substantially tracks changes in process, temperature and voltage.

19. (currently amended) A locked loop, comprising:

a first circuit path having a plurality of stages each having a variable amount of drive associated therewith;

a second circuit path in series with said first circuit path and having a plurality of stages each having at least a fast and a slow path;

a control circuit for controlling the number of stages in said first circuit path and the number of ~~stages~~ fast paths and slow paths in said second circuit path;

a phase detector for producing signals for input to said control circuit; and

a feedback path for connecting an output of said first circuit path to an input of said second circuit path and said phase detector.

20. (original) The locked loop of claim 19 wherein said first circuit path has an intrinsic delay smaller than the intrinsic delay of said second circuit path.

21. (original) A dual locked loop, comprising:

a first locked loop for establishing a phase relationship between an output signal and a reference signal;

a second locked loop responsive to said first locked loop and comprising:

a delay line having a first portion providing a variable amount of delay substantially independently of process, temperature and voltage variations and a second portion in series with said first portion and providing a variable amount of delay that substantially tracks changes in process, temperature, and voltage variations;

a control circuit for controlling the delay of said delay line;

a phase detector for producing signals for input to said control circuit; and

a feedback path for connecting an output of said delay line to an input of said first locked loop and to said phase detector, said output signal being available at said output of said delay line.

22. (original) The dual locked loop of claim 21 wherein said first portion of said delay line has a small intrinsic delay and said second portion of said delay line has a higher intrinsic delay than said first portion.

23. (original) The dual locked loop of claim 21 wherein in said first portion of said delay line the delay is varied by varying the load and in said second portion of said delay line the delay is varied by selecting a desired signal path.

24. (original) The dual locked loop of claim 23 wherein the desired signal path is one of a slow path and a fast path.

25. (original) The dual locked loop of claim 23 wherein the desired signal path is one of a series path through an inverter and a parallel path through inverters.

26. (original) A dual locked loop, comprising:

a first locked loop for establishing a phase relationship between an output signal and a reference signal;

a second locked loop responsive to said first locked loop and comprising:

a delay line having a first portion providing a variable amount of delay with little intrinsic delay and a second portion providing a variable amount of delay with a larger intrinsic delay;

a control circuit for controlling the delay of said delay line;

a phase detector for producing signals for input to said control circuit; and

a feedback path for connecting an output of said delay line to an input of said first locked loop and to said phase detector, said output signal being available at said output of said delay line.

27. (original) The dual locked loop of claim 26 wherein the delay of said first portion of said delay line is substantially independent of process, temperature and voltage variations and wherein the delay of the second portion of the delay line substantially tracks changes in process, temperature and voltage variations.

28. (original) The dual locked loop of claim 26 wherein in said first portion of said delay line the delay is varied by varying the load and in said second portion of said delay line the delay is varied by selecting a desired signal path.

29. (original) The dual locked loop of claim 28 wherein the desired signal path is one of a slow path and a fast path.

30. (original) The dual locked loop of claim 28 wherein the desired signal path is one of a series path through an inverter and a parallel path through inverters.

31. (original) A dual locked loop, comprising:

a first locked loop for establishing a phase relationship between an output signal and a reference signal;

a second locked loop responsive to said first locked loop and comprising:

a first circuit path having a stepwise variable capacitive load;

a second circuit path in series with the first circuit path and having a plurality of stages each having at least two paths;

a control circuit for controlling the amount of capacitance in said first circuit path and the number of stages in said second circuit path;

a phase detector for producing signals for input to said control circuit; and

a feedback path for connecting an output of said second locked loop to an input of said first locked loop and to said phase detector, said output signal being available at said output of said second locked loop.

32. (original) The dual locked loop of claim 31 wherein said first circuit path has an intrinsic delay smaller than the intrinsic delay of said second circuit path.

33. (original) The dual locked loop of claim 31 wherein said first circuit path is substantially independent of process, temperature and voltage variations while said second circuit path substantially tracks changes in process, temperature and voltage.

34. (original) The locked loop of claim 31 wherein the two paths include a fast and a slow path.

35. (original) The locked loop of claim 31 wherein the two paths include a series path through an inverter and a parallel path through inverters.

36. (original) A dual locked loop, comprising:

a first locked loop for establishing a phase relationship between an output signal and a reference signal;

a second locked loop responsive to said first locked loop and comprising:

a first circuit path having a stepwise variable capacitive load and a second circuit path having a plurality of stages each having a variable amount of drive associated therewith;

a control circuit for controlling the amount of capacitance in said first circuit path and the number of stages in said second circuit path;

a phase detector for producing signals for input to said control circuit; and

a feedback path for connecting an output of said second locked loop to an input of said first locked loop and to said phase detector, said output signal being available at said output of said second locked loop.

37. (original) The dual locked loop of claim 36 wherein said first circuit path has an intrinsic delay smaller than the intrinsic delay of said second circuit path.

38. (original) The dual locked loop of claim 36 wherein said first circuit path is substantially independent of process, temperature and voltage variations while said second circuit path substantially tracks changes in process, temperature and voltage.

39. (currently amended) A dual locked loop, comprising:

a first locked loop for establishing a phase relationship between an output signal and a reference signal;

a second locked loop responsive to said first locked loop and comprising:

a first circuit path having a plurality of stages each having a variable amount of drive associated therewith and a second circuit path in series with said first circuit path and having a plurality of stages each having at least a fast and a slow path;

a control circuit for controlling the number of stages in said first circuit path and the number of ~~stages~~ fast paths and slow paths in said second circuit path;

a phase detector for producing signals for input to said control circuit; and

a feedback path for connecting an output of said second circuit to an input of said first circuit and to said phase detector.

40. (original) The dual locked loop of claim 39 wherein said first circuit path has an intrinsic delay smaller than the intrinsic delay of said second circuit path.

41. (currently amended) A method of operating a locked loop, comprising:

propagating a signal through two different types of variable delay circuits, a first ~~one~~ circuit being substantially independent of process, temperature and voltage variations and a second ~~one~~ circuit tracking changes in process, temperature and voltage variations;

feeding back the propagated signal to the input of one of the delay circuits and a phase detector; and

detecting a phase difference between said feedback signal and a reference signal to produce control signals for said first and second delay circuits.

42. (currently amended) A method of operating a locked loop, comprising:

propagating a signal through two different types of series-connected delay circuits, one circuit ~~have~~ having a small intrinsic delay and the other circuit having a larger intrinsic delay;

feeding back the propagated signal to the input of one of the delay circuits and a phase detector; and

detecting a phase difference between said feedback signal and a reference signal to produce control signals for said delay circuits.

43. (currently amended) A method of operating a locked loop, comprising:

propagating a signal through a first circuit path having a stepwise variable capacitive load;

propagating said signal through a second circuit path in series with said first circuit path and having a plurality of stages each having at least two paths;

feeding back the propagated signal to the input of the first circuit path and a phase detector; and

detecting a phase difference between said feedback signal and a reference signal to produce control signals for said first and second circuit paths.

44. (currently amended) A method of operating a locked loop, comprising:

propagating a signal through a first circuit path having a stepwise variable capacitive load;

propagating said signal through a second circuit path in series with said first circuit path and having a plurality of stages each having a variable amount of drive associated therewith;

feeding back the propagated signal to the input of the first circuit path and a phase detector; and

detecting a phase difference between said feedback signal and a reference signal to produce control signals for said first and second circuit paths.

45. (currently amended) A method of operating a locked loop, comprising:

propagating a signal through a first circuit path having a plurality of stages each having a variable amount of drive associated therewith;

propagating said signal through a second circuit path in series with said first circuit and having a plurality of stages each having at least a fast and a slow path;

feeding back the propagated signal to the input of the first circuit path and a phase detector; and

detecting a phase difference between said feedback signal and a reference signal to produce control signals for said first and second circuit paths.

46. (currently amended) A method of operating a dual locked loop, comprising:

propagating a signal through a first locked loop to establish a phase relationship between an output signal and a reference signal;

propagating said signal through two different types of variable delay circuits, a first ~~one~~ circuit being substantially independent of process, temperature and voltage variations and a second ~~one~~ circuit tracking changes in process, temperature and voltage variations;

feeding back the propagated signal to the input of the first locked loop and a phase detector; and

detecting a phase difference between said feedback signal and a reference signal to produce control signals for said first and second delay circuits.

47. (currently amended) A method of operating a dual locked loop, comprising:

propagating a signal through a first locked loop to establish a phase relationship between an output signal and a reference signal;

propagating said signal through two different types of delay circuits, one circuit having ~~have~~ a small intrinsic delay and the other circuit having a larger intrinsic delay;

feeding back the propagated signal to the input of the first locked loop and a phase detector; and

detecting a phase difference between said feedback signal and a reference signal to produce control signals for said delay circuits.

48. (currently amended) A method of operating a dual locked loop, comprising:

propagating a signal through a first locked loop to establish a phase relationship between an output signal and a reference signal;

propagating said signal through a first circuit path in series with said first locked loop and having a stepwise variable capacitive load;

propagating said signal through a second circuit path in series with said first circuit path and having a plurality of stages each having at least two paths;

feeding back the propagated signal to the input of the first locked loop and a phase detector; and

detecting a phase difference between said feedback signal and a reference signal to produce control signals for said first and second circuit paths.

49. (currently amended) A method of operating a dual locked loop, comprising:

propagating a signal through a first locked loop to establish a phase relationship between an output signal and a reference signal;

propagating said signal through a first circuit path having a stepwise variable capacitive load;

propagating said second signal through a second circuit path in series with said first circuit path and having a plurality of stages each having a variable amount of drive associated therewith;

feeding back the propagated signal to the input of the first locked loop and a phase detector; and

detecting a phase difference between said feedback signal and a reference signal to produce control signals for said first and second circuit paths.

50. (currently amended) A method of operating a dual locked loop, comprising:

propagating a signal through a first locked loop to establish a phase relationship between an output signal and a reference signal;

propagating said signal through a first circuit path having a plurality of stages each having a variable amount of drive associated therewith;

propagating said signal through a second circuit path in series with said first circuit path and having a plurality of stages each having at least fast and slow paths;

feeding back the propagated signal to the input of the first locked loop and a phase detector; and

detecting a phase difference between said feedback signal and a reference signal to produce control signals for said first and second circuit paths.